IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael A Vyvoda et al.

Title: Wafer Surface that Facilitates Particle Removal

Docket No.: MA-027
Filed: February 2, 2001
Examiner: Anh D. Mai

Serial No.: 09/776,009
Due Date: ~~September 18, 2005~~
Group Art Unit: 2814

MS Appeal Brief
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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X A Brief on Appeal (11 Pages).

By: _____
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. MA-027

In re patent application of
Michael A. Vyvoda et al.

Serial No. 09/776,009 Group Art Unit: 2814

Filed: February 2, 2001 Examiner: Anh D. Mai

For: WAFER SURFACE THAT FACILITATES PARTICLE REMOVAL

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 9, 2005

To the Commissioner:

In this Appeal Brief, Appellants hereby appeal the January 7, 2005 final rejection of claims 63-66 and 68-70 in the above-identified application to the Board of Patent Appeals and Interferences.

This Appeal Brief is resubmitted in response to a Notice of Non-Compliant Appeal Brief. The required Evidence and Related Proceedings appendices have been included.

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Pamela J. Squyres, reg. no. 52,246

9/9/05
Date of Deposit

I. REAL PARTY IN INTEREST

The real parties in interest are, jointly, Matrix Semiconductor, Inc., a Delaware corporation, and LSI Logic Corporation, a Delaware corporation.

II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of other related appeals and interferences.

III. STATUS OF CLAIMS

Claims 63-66 and 68-70 are pending in the Application. Claims 63-66 and 68-70 have been rejected and are the subject of this appeal. A listing of the appealed claims is presented in the APPENDIX.

IV. STATUS OF AMENDMENTS

No amendments after final rejection were filed.

V. SUMMARY OF INVENTION

Chemical mechanical planarization (CMP) is a process used during fabrication of semiconductor devices. Layers can be deposited above a wafer substrate, then subjected to other process such as pattern and etch. Performing CMP on these layers produces a substantially planar surface. Residual slurry particles and metals may become exposed on the surface of the wafer after the CMP step is completed. These slurry particles and metals should be removed to avoid contamination. A previously known cleaning technique removes the residual particles by placing the wafer in a scrubber in which dilute (e.g., about 2%) aqueous ammonium hydroxide (NH_4OH) is administered to the wafer surface while polyvinyl alcohol (PVA) brushes physically remove the residual slurry particles and metals. The surface of the wafer must be hydrophilic (i.e., attracts water) so that the wafer easily wets when placed in the aqueous environment within the scrubbing tool. When the wafer

successfully wets, the PVA brushes can come into intimate contact with residual particles on the wafer surface and effect their removal.

This aqueous cleaning technique has been used to remove residual slurry particles from a silicon dioxide dielectric surface following CMP and to remove residual slurry particles from a combined silicon dioxide and silicon nitride dielectric surface following shallow trench isolation (STI) planarization. Both silicon dioxide and silicon nitride are hydrophilic. However, when silicon is exposed following a CMP process, a hydrophobic (i.e., water-repelling) surface is created, which makes it difficult to use aqueous NH_4OH-based scrubbing. The silicon surface does not sufficiently wet to permit the PVA brushes from coming into intimate contact with the wafer surface, and the residual slurry particles and/or metal contaminants are not removed.

In the present invention, regions of hydrophobic material (such as silicon) and hydrophilic material (such as dielectric) are exposed at a wafer surface after a CMP removal process. In the present invention it has been found that the size, shape, and proportion of the hydrophobic and hydrophilic regions can be arranged to improve wettability, and thus cleanability, of the post-CMP surface.

In the present invention, the silicon and dielectric regions are arranged so that the overall area of the wafer that is hydrophobic (silicon) is not above a critical proportion, and that at no point on the wafer is there an uninterrupted expanse of hydrophobic material (silicon) which is too large. So long as the silicon and dielectric regions are arranged as described in the present invention, the entire wafer surface can wet sufficiently to allow post-CMP cleaning by conventional methods.

VI. ISSUES

The sole issue presented in this appeal is whether claims 63-66 and 68-70 are anticipated by Wu, US Patent No.6,008,087, under 35 USC 102(e), or, in the alternative, unpatentable over Wu under 35 USC 103(a).

VII. GROUPING OF CLAIMS

The rejected claims stand and fall together.

VIII. ARGUMENT

The only independent claim among the appealed claims is claim 63. Claim 63 recites a wafer having a surface, the surface comprising: a plurality of elongated strips of polysilicon; and a plurality of elongated strips of dielectric material, the strips of dielectric material alternating with the strips of polysilicon, wherein the surface has been planarized by chemical mechanical planarization, and wherein a first percentage of total wafer surface area that is polysilicon is less than or equal to 70 percent. *Polysilicon* is polycrystalline silicon, and is hydrophobic.

In Fig. 6 and related description, Wu does apparently teach alternating elongated strips of dielectric material (oxide 20) and polysilicon (16) at a surface planarized by chemical mechanical planarization.

Claim 63, however, goes on to recite that the percentage of the total wafer surface area that is polysilicon is less than or equal to 70 percent. The Examiner asserts that such a percentage is taught by Wu, apparently relying for these percentages on Figs. 6 and 9.

Drawings with no scale cannot be relied upon for such evidence, however. To assume the relative widths of the polysilicon strips 16 and oxide 20 (and from those relative widths to infer their relative percentage of total surface area) from a subjective estimate of their

appearance in Fig. 6, for example, in the absence of an explicit teaching, is improper. Referring to MPEP 2125:

> When the reference does not disclose that the drawings are to scale and is silent as to dimensions, arguments based on measurement of the drawing features are of little value.

MPEP 2125 continues, quoting from *Hockerson-Halberstadt, Inc. v Avia Group Int'l*, 222 F.3d 951, 956, 55 USPQ2d 1487, 1491 (Fed. Cir. 2000):

> "[I]t is well established that patent drawings do not define the precise proportions of the elements and may not be relied on to show particular sizes if the specification is completely silent on the issue."

Wu discloses a wide range of possible widths for polysilicon lines 16 (between about 200 to about 3000 angstroms, col. 3, lines 51-55.) The possible width of dielectric lines 20 is more difficult to determine, as dielectric 20 fills two sets of gaps formed in two separate steps. Referring to Fig. 4 of Wu, each silicon nitride structure 6 is between 300 and 3000 angstroms wide (col. 3, line 36-37). Each silicon nitride structure (portion) 6 is then removed, as shown in Fig. 5, forming the first set of gaps, each of which is filled by dielectric 20, in Fig. 6. Another set of gaps 12, between portions 6 in Fig. 3, is between 500 and 5000 angstroms wide (col. 3, lines 38-39). These gaps are partly filled by polysilicon 16 (shown in Fig. 4), then the remainder of the gap filled by dielectric 20 (Fig. 6).

What, then, is the percent surface area of Wu's wafer surface that is polysilicon? The answer is unknown. Some combinations of disclosed dimensions yield 70 percent polysilicon or less within the area shown in Fig. 6 while others do not. (Further, Wu is silent regarding the portion of the wafer *outside* of the area shown in Fig. 6, and it is the percentage of the surface area of the *entire* wafer that is claimed.)

Simply put, if the surface area of the wafer that includes the resulting surface, shown in Fig. 6, can unambiguously be shown to be 70 percent silicon or less, then Wu does indeed anticipate claim 63. If it is merely *possible* that the surface area of this wafer is 70 percent

silicon or less, but no clear teaching to this effect exists, then Wu does not anticipate claim 63.

The Examiner argues that because some combinations of the dimensions disclosed in Wu *could* yield a polysilicon percentage area of 70 percent or less, these combinations must be considered to have been disclosed, and therefore Wu anticipates. This cannot be supported.

By way of analogy, consider a novel mortar-and-pestle combination. Suppose it were discovered that when a pestle made of granite is used with a mortar made of teak, the granite-and-teak combination has unexpectedly superior grinding qualities when used to grind coffee beans, which have presented difficulty because of their high oil content. The advantageous interaction is taught, and grinding of coffee beans using a granite-pestle-and-teak-mortar combination is claimed. A reference is found teaching a pestle made of any of several materials, including granite, slate, marble, oak, steel, or ivory. The pestle can be used with a mortar, which may be made of any suitable material; agate, concrete, mica, teak, and porcelain are mentioned. The mortar and pestle of the reference can be used for general grinding, and the particular problems presented by coffee beans are not mentioned. No particular pairing is preferred over any other. The reference makes no mention of the unexpected properties of the granite-pestle-and-teak-mortar combination.

The reference does not anticipate the claim of a granite pestle and teak mortar used to grind coffee beans. The granite-teak combination is central to the claim, but is neither explicitly taught nor suggested by the reference, which doesn't even recognize the problem to be solved. That it is *possible* to arrive at this particular combination from the disclosure of the reference goes beyond the actual teaching of the reference, and is improper.

Returning to the present invention, only certain combination of a subset of disclosed widths of polysilicon lines 16 and dielectric lines 16 of Wu yield the 70 percent or less surface area required by the claim. Wu is silent regarding the relative widths (and thus the relative surface area) of each material, and does not address or appear to recognize the problem of cleaning a post-CMP surface exposing hydrophobic material. Wu discloses dimensions, but does not disclose the *combination* of dimensions required to render such a post-CMP surface cleanable, and thus does not anticipate claim 63.

Accordingly, Appellants respectfully request that the rejections of claims 63 and its dependent claims 64-66 and 68-70 be withdrawn.

CONCLUSION

Accordingly, Appellants respectfully solicit the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

Sept. 9, 2005

Date

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This Appeal Brief is hereby RESUBMITTED to correct defects. The appeal fee has already been paid by applicants. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 502302.

IX. CLAIMS APPENDIX

1-62. (Cancelled)

63. A wafer having a surface, the surface comprising:

a plurality of elongated strips of polysilicon; and

a plurality of elongated strips of dielectric material, the strips of dielectric material alternating with the strips of polysilicon,

wherein the surface has been planarized by chemical mechanical planarization, and

wherein a first percentage of total wafer surface area that is polysilicon is less than or equal to 70 percent.

64. The wafer of claim 63 wherein the first percentage is greater than 50 percent.

65. The wafer of claim 63 wherein the first percentage is less than or equal to 60 percent.

66. The wafer of claim 65 wherein the first percentage is greater than 50 percent.

67. (Cancelled)

68. The wafer of claim 63 wherein the strips of polysilicon have a shortest dimension less than or equal to 500 microns.

69. The wafer of claim 68 wherein the strips of polysilicon have a shortest dimension between 0.25 and 500 microns.

70. The wafer of claim 63 wherein the surface of the wafer can attract enough water to wet sufficiently allowing removal of residual particles therefrom.

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.